EXHIBIT A

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MOTOROLA

Bar Date: June 2000 !

CONFIDENTIAL PROPIETARY

MOTOROLA PATENT COMMITTEE

MOTOROLA INC
[redacted]
AUSTIN INTELLECTUAL PROPERTY DEPARTMENT

DISCLOSURE FOR PATENT COMMITTEE
SUBMITTED PURSUANT TO EMPLOYMENT AGREEMENT.

FOR INSTRUCTIONS FOR COMPLETION CONTACT
PATENT COMMITTEE MEMBER IN YOUR ORGANIZATION

1/94 **PLEASE SEND TWO (2) COPIES**

Inventor(s) will not fill in

DIVISION NCSG

DISCLOSURE NO. DATE 9/051

COMMITTEE: (INVENTOR MAY SELECT)

- ☐ Circuits/Packaging
- ☐ Process
- ☒ Systems/Software

Inventors must fill in all items 1 to 14. (PLEASE PRINT OR TYPE)
ITEMS 2 TO 4 MAY REQUIRE EXTRA SHEETS. BE SURE THEY ARE SIGNED, WITNESSED AND ATTACHED.

1. Name of the invention. (limit to ten words) Estimation of Maximum and Average Leakage Power in MOS ICs

2. What are the problems solved by this invention? see attached sheets

3. Give a complete description of the invention, including its operation, purpose and environment. (Use separate sheets). see attached sheets

4. What improvement over known technology is accomplished by this invention? see attached sheets

5. List the closest known technology (e.g. publication, patent or commercial product) providing the same or similar results: "Estimation of Standby Leakage Power in CMOS Circuits Considering Accurate Modeling of Transistor Stacks," ISLPED-98

6. What new elements (e.g. components, circuits, process steps) or combinations of known elements or software algorithm produced the improvement? A new method for estimating maximum and average leakage power.

7. What are the potential applications for use of this invention? Low power, high performance micro processors, micro-controllers and circuit designs.

8. What was the conception date? [redacted] (Attach pertinent log sheets, drawings,etc., to support dates. Always attach the earliest drawing and the earliest written description.) See attached sheets

9. To whom did you first disclose this invention? Name: Gopal Vijayan Date [redacted]

10. When was the device first built and tested? Date? [redacted] Motorola
State the present location of the device.

DETERMINATION OF LEGAL INVENTORSHIP FOR PATENT APPLICATION MUST BE MADE BY THE INTELLECTUAL PROPERTY DEPARTMENT.

Inventor's signature (IMPORTANT - YOU MUST USE YOUR FULL NAME) - NO INITIALS -

11. Inventors Name: Supamas Sirichotiyakul Signature: Supamas Sirichotiyakul Date: [redacted]

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Panda X4462 Rblaauw

Tim Edwards x7372 - On one

T THEY UNDERSTAND THE

_____ Date: [redacted]

_____ Date: [redacted]

Items 18 to 26 are to be filled in by the ENGINEERING MANAGER, LABORATORY MANAGER or above.
THE MANAGER IN SIGNING THIS FORM ATTESTS TO THE FACT THAT THE MANAGER UNDERSTANDS THE INVENTION.

18. What product will this invention be used in? (No codes names - use brief description if necessary)
Invention will be used in design of Motorola digital ICs.

19. When is the estimated shipping date? Not Applicable

20. When (was)(will) the first offer for sale of a product incorporating this invention (be) made?
Date: Not applicable

21. When (was)(will) the first disclosure outside of Motorola (be) made? Planed for DATE conference,
How and to whom? State title and date of publication, if any. submission date: [redacted]

22. What is the market for products incorporating this invention? Microprocessors and microcontroller

23. Who are the potential competitors: Internal CAD organizations within Motorola competitors

24. Did this invention result from work on a development Contract? (YES)(NO) Contract No. No
Who was the contracting party?

25. Discuss the business impact that this invention will have on Motorola. Provide accurate measurement of maximum and average leakage power of Motorola digital ICs.

26. Manager's Name: Bill Read Signature: _____ Date: [redacted]
Phone: 794-4021
Dept. No.: RM532

Witness Signature: _____ Date: [redacted]
Witness Signature: _____ Date: [redacted]

2. Problems Solved

Increase usage of battery operated devices has created a greater need for circuits with very low static leakage current. More stringent specifications are being placed on the amount of leakage power drawn while a device is in the stand-by mode. The leakage power consideration has become even more important in the deep sub-micron and sub-1V circuits. In such cases, a low threshold voltage device is required to maintain performance, which results in high subthreshold leakage power. As a result a careful trade-off between performance and leakage power has become essential. In making such a trade-off, an accurate estimation of leakage power is needed. Subthreshold leakage power is the most dominant component in leakage power dissipation. In this patent, we propose a new method to efficiently estimate maximum and average subthreshold leakage power dissipation in MOS digital circuits.

3. Description

The subthreshold leakage power estimation proposed involves the following steps. First all dominant leakage states of each DC-connected component are identified. Subthreshold leakage power is highly dependent on the circuit state in stand-by mode. In real application the circuit state for stand-by mode can be partially unknown or even fully unknown. A dominant leakage state is defined as a state which can contribute significant amount of leakage power in the circuit. Non-dominant leakage states are guaranteed to have much less leakage power than dominant states and can be ignored in the calculation. The dominant leakage states are identified using a modified cutset finding algorithm, graph reduction techniques, and a greedy approach in assigning the remaining unknown input states in the reduced graph. In the next step, a simple DC analysis is done for the reduced graph of each dominant state to calculate the subthreshold leakage power of that state. Then, the maximum and average subthreshold leakage power of the DC-connected component is calculated from these dominant state leakage power using state probabilities. The maximum and average circuit leakage power is then obtained by the summation of all DC-connected components' maximum and average leakage power.

4. Improvements Over Known Technology

Our method provides a new approach to estimate both maximum and average leakage power in a fast and accurate fashion. This approach is novel in that it determines the dominant states needed for DC analysis. Generally, the number of dominant states is much smaller than the number of all possible states which is exponential with the number of input. It also utilizes state probability in the calculation to provide a more accurate estimation.

#91057

Estimation of Average Leakage Power in MOS ICs

Inventors: Supamas Sirichotiyakul, David Blaauw, Tim Edwards, Chanhee Oh, Rajendran Panda, Abhijit Dharchoudhury

Project: **Duet:** Leakage power estimation and optimization tool

Customer: MSIL Quartz

Presentation Overview:

- Definition of the Problem
- Prior Art
- Specific Claims
- Results
- Uniqueness
- Usefulness and Competitive Advantage

Definition of the Problem

Motivation:

Leakage power is important for portable application:

- Circuit is in standby mode most of the time
- Leakage power consumed during standby modes
- Battery life mainly determined by average leakage power consumption

=> Leakage power is a design constraint

Design trends: lower power supply and smaller threshold voltage devices -> higher leakage

Motorola puts more emphasis on wireless market

The problem:

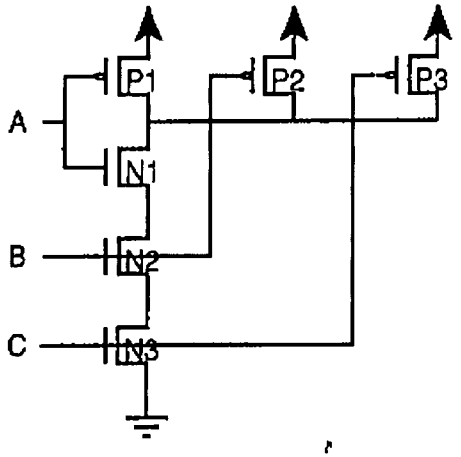
How can we estimate average leakage power accurately and quickly?

Difficulties:

- Leakage power depends on the circuit state in standby mode which is usually random or partially random.
- Average leakage power must be calculated over all possible standby mode circuit states. The number of these states increases exponentially with the number of input signals.

State Dependency

Example: 3-input NAND gate



State (ABC)	Leakage Current (nA)
000	0.098441
001	0.187332
010	0.187455
011	1.065310
100	0.179789
101	0.813584
110	0.783156
111	5.321400

Prior Art

What designers have been doing:

Use the number of transistors in a circuit to predict the average leakage power

- Extremely inaccurate
- Only useful for early chip-level estimation

Brute force method: Run Spice simulations of all possible standby mode circuit states.

- 2^n simulations for n unknown input signals, infeasible for large n

Patents/Publications:

ISLPED'98 Paper by Z. Chen, et al.

- Only estimates maximum leakage power, not average leakage power
- Maximum leakage power is a poor prediction of battery life

No other approaches found in GIC database searches.

- Keywords: "standby power estimation" "leakage power estimation" "leakage current estimation"

Known alternatives to the proposed method: None

Average Leakage Current Estimation

1. Divide circuit into gates
2. Calculate signal probability, pairwise signal correlation of gate input signals
3. For each gate:
   - 3.1 Find cutsets — Graph traversal
   - 3.2 For each cutset:
     - 3.2.i. Find dominant states — Graph reduction; Greedy Algorithm
   - 3.3 For each dominant state:
     - 3.3.i. Calculate leakage current — Graph reduction; Non-linear solver - Newton-Raphson
     - 3.3.ii. Calculate state probability — Pairwise signal correlation
   - 3.4 Calculate gate average leakage — average leakage(gate) = $\Sigma_{\text{all states}}$ prob(state)*leakage(state)
4. Calculate circuit average leakage — average leakage(circuit) = $\Sigma_{\text{all gates}}$ average leakage(gate)

Claims: Overall flow, Step 3.1, Step 3.2.i.

Dominant States

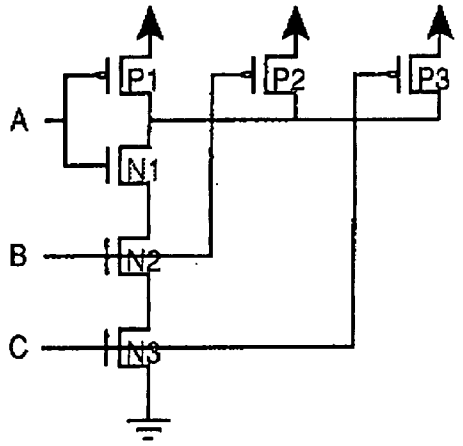


Table 1: Leakage Current of a 3-input NAND Gate

State (ABC)	Leakage Current (nA)	Leaking Transistors
000	0.098441	N1, N2, N3
001	0.187332	N1, N2
010	0.187455	N1, N3
011	1.065310	N1
100	0.179789	N2, N3
101	0.813584	N2
110	0.783156	N3
111	5.321400	P1, P2. P3

- Dominant states are states of a gate that have high leakage, only one transistor is off in any Vdd-Gnd path. Other states are guaranteed to have significantly lower leakage and can be ignored.
- We discovered that the set of dominant states are the cut-sets of the transistor graph where Vdd is in one partition and Gnd is in the other.

Average Leakage Current Estimation Results

Circuit	Number of Inputs	Number of Circuit States	Number of Solve States / Dominant States	Leakage Results			Runtime	
				Spice (nA)	Ours (nA)	Accuracy (%)	Spice	Ours
blk	9	512	30 / 78	9.492130	9.21834	2.88	6 min. 15 sec.	< 1 sec.
bay	9	512	16 / 52	3.565960	3.32067	6.88	6 min. 12 sec.	1 sec.
add1	10	1024	71 / 171	23.24950	22.1327	4.80	35 min. 35 sec.	1 sec.
pla	12	4096	246 / 809	160.0240	142.008	11.26	3 hr. 27 min.	2 sec.
add2	51	2.25 e15	270 / 646	NA	28.0672	NA	NA	2 sec.

Uniqueness

- Avoid exponential complexity:
  - Use weighted gate based average leakage calculation.
  - The number of states in each gate is reduced significantly by determining only leakage dominant states.
- Incorporates state probability to provide a more accurate average of leakage power.
- Very good accuracy with extremely fast run time.
- Can be used as a part of leakage optimization engine.
- Allows average leakage analysis on large circuits that cannot be done previously.
- No leakage power estimation tool available from CAD vendors.

Usefulness

- The proposed algorithm gives an accurate estimation of average leakage power without running a large number of Spice simulations.
  - Higher confidence level in design sign-offs
  - Allows designers to make well-informed decision on design trade-offs on high leakage blocks
  - Leakage budgeting
  - Engine for leakage optimization tool

Competitive Advantage to Motorola

- Products that will use this invention:
  - MSIL Quartz
  - PowerPC and MCore is investigating the software
  - Portable sub-1V chip
- Competitors who can use this invention: TI, IBM, Lucent